

Task Force on Fault Current Limiter Testing Sponsored by IEEE Switchgear ADSCOM

2009 IEEE/PES Joint Technical Meeting January 15th, 2009 Minutes Atlanta, GA

Frank Lambert called the first meeting of the Task Force to order at 10:30 AM with 9 members and guests present.

1. Introductions of the attendees were made including their interest and experience in FCL testing.
2. Frank Lambert provided an overview of the background, planned scope and approach to develop the guide for testing novel FCL technologies (presentation attached).
3. Mischa Steurer (steuerer@caps.fsu.edu) was elected TF chair and Frank Lambert (frank.lambert@neetrac.gatech.edu) was elected Secretary.
4. The IEEE required slides on Patents for Working Groups were discussed. Members were advised to abide by these requirements.
5. CIGRE WG A3.23, "Application and feasibility of fault current limiters in power systems", will hold their next meeting March 9 – 10 in Los Angeles, CA. The convener of the CIGRE WG, Heino Schmitt granted permission to allow guests to attend this meeting. Please contact Heino Schmitt (heino.schmitt@siemens.com) or Mischa Steurer (steuerer@caps.fsu.edu) for details.
6. The TF next meeting will be held in conjunction with the Switchgear Committee Meeting in Asheville, N.C. on Wednesday, May 6th. Representatives of each of the FCL technologies will be asked to provide a description of their technology and specific recommendations for testing in as much detail as possible. So far, the team has identified the following technologies and developers to be asked to contribute:

Technology	Developer
<i>Superconducting</i>	
Shielded core	Areva
Saturable iron core	Zenergy Power
Resistive w/ external shunt reactor	Siemens / American Superconductor
Resistive w/ internal shunt reactor	SuperPower
Resistive w/o shunt reactor	Nexans
FCL HTS Cable	American Superconductor / Southwire
<i>Power Electronics</i>	
SGTO w/ internal shunt reactor	Silicon Power Corporation

7. Robert Dommerque made a presentation on testing requirements for a 12 kV Fault Current Limiter (presentation attached).
8. A draft PAR will be developed for review at the next meeting.

The meeting was adjourned at 12:10 PM.

Submitted by:
Frank Lambert

New IEEE Task Force on Fault Current Limiter Testing

Frank C. Lambert
Georgia Tech - NEETRAC



&

Michael „Mischa“ Steurer
*Center for Advanced Power Systems,
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*Presented at the 1st meeting of the new IEEE TF
Atlanta, GA, Jan 15, 2009*

Business during the 1st meeting

- Introduction
- New TF – goal, scope, approach
- Election of
 - Chairman
 - Vice chairman
 - Secretary
- Assignments
 - ftp site for information and literature
 - Document chapter responsibilities according to approach
- Next meeting
 - Next regular meeting of the IEEE Switchgear Committee will be in Asheville, NC, May 3 – 7, 2009
 - Presentations?
 - Draft PAR for review

New IEEE Task Force

- Goal
 - Develop a guide for testing novel FCL technologies (SC and non-SC)
 - Complements activities by CIGRE WG-A3.23
- Scope
 - Identify FCL testing requirements from a utility point of view
 - Identify specific testing needs regarding the different FCL technologies (e.g. superconducting vs. power electronics)
 - Identify applicability of existing power equipment testing standards
 - Recommend additional tests and testing procedures as needed
 - Identify gaps in availability of testing capabilities and recommend power requirements for upgrading

New IEEE Task Force

- Approach
 - Study and review novel fault current limiter (FCL) technologies for medium and high voltage systems.
 - Map testing requirements against the needs by different FCL technologies
 - Map testing requirements against existing power equipment testing standards
 - Map testing requirements against available laboratory capabilities
 - Coordinate with other technical committees, groups, societies and associations as required
- Status
 - New IEEE task force was approved by the IEEE Switchgear Committee in October 2008
 - **For writing a standard we need a Project Authorization Request (PAR)**

Superconducting Fault Current Limiter to Applied Superconductor Ltd.



Superconducting Fault Current Limiter to Applied Superconductor Ltd.

Design specifications

- rated voltage $U_r = 12\text{kV}$
- rated current $I_r = 100\text{A}$
- inrush current $I = 460\text{A} (10\text{s})$
- prospective current $I''_k = 22\text{kA} (R/X=0,8)$
- first peak limiting $i_p < 6\text{kA}$
- limitation time $t = 120\text{ms}$
- total loss $P = 230\text{W}$
- operating temperature $T = 73\text{K}$

Test specifications

- Withstand voltage $U_w = 28\text{kV}$
- Partial discharge $P < 5\text{pC}$
- Lightning impulse (15 repetitions) $U_{+/-} = 95\text{kV}$
- 3 times 100% prospective fault current
- 3 times 60% prospective fault current
- 3 times 30% prospective fault current
- 3 times 10% prospective fault current

